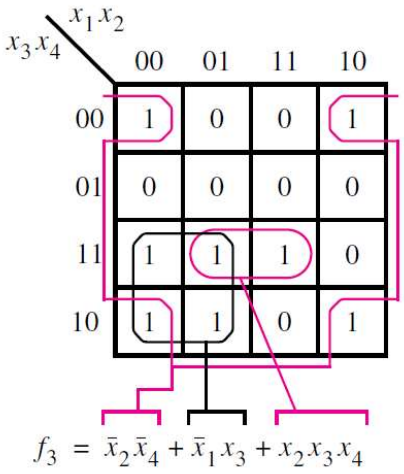
EMTR-2011: Microcontrollers and Digital Logic
Assignment 2 Reference Solution

Question 1

Construction the Karnaugh maps based on the following truth tables and derive the circuit outputs.

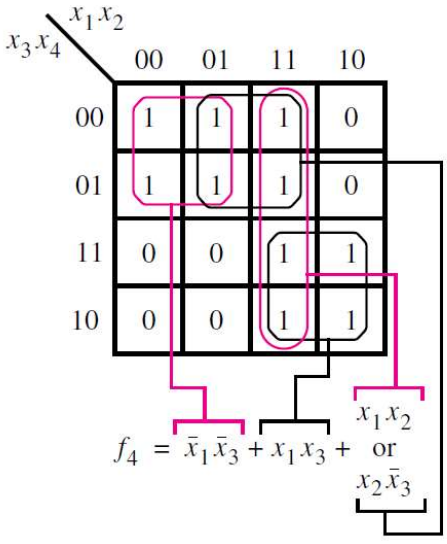
(a)

x_1	x_2	x_3	x_4	f
0	0	0	0	1
0	0	0	1	0
0	0	1	1	1
0	0	1	0	1
0	1	0	0	0
0	1	0	1	0
0	1	1	1	1
0	1	1	0	1
1	0	0	0	1
1	0	0	1	0
1	0	1	1	0
1	0	1	0	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1



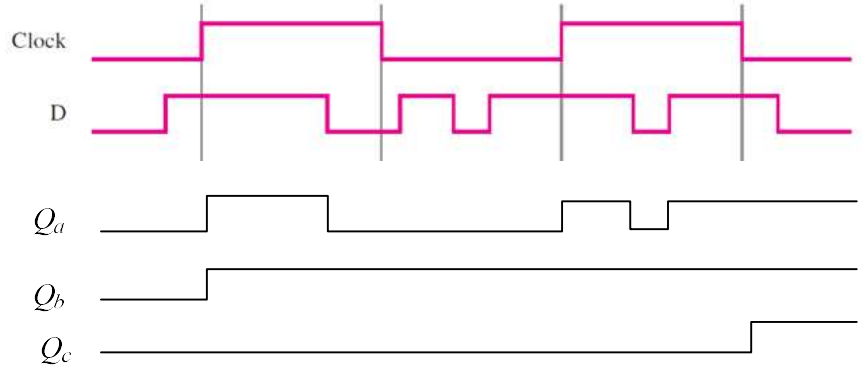
(b)

x_1	x_2	x_3	x_4	f
0	0	0	0	1
0	0	0	1	1
0	0	1	1	0
0	0	1	0	0
0	1	0	0	1
0	1	0	1	1
0	1	1	1	0
0	1	1	0	0
1	0	0	0	0
1	0	0	1	0
1	0	1	1	1
1	0	1	0	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1



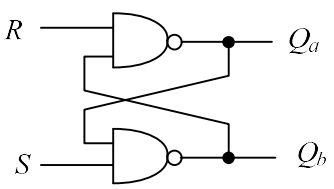
Question 2: Problem 5.1

Consider the timing diagram in Figure P5.1. Assuming that the *D* and *Clock* inputs shown are applied to the circuit in Figure 5.10, draw waveforms for the Q_a, Q_b, and Q_c signals.

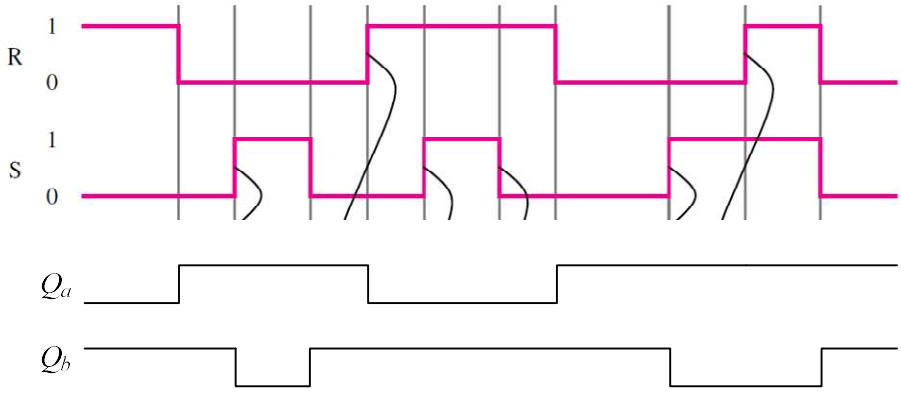


Question 3: Problem 5.2

Figure 5.4 shows a latch built with NOR gates. Draw a similar latch using NAND gates. Derive its characteristic table and show its timing diagram.



S	*R*	Q_a	Q_b	
0	0	1	1	
0	1	0	1	
1	0	1	0	
1	1	1/0	0/1	(no change)



Question 4:

(a) Problem 1-12

The ROM area is where the executable code is stored.

(b) Problem 1-29

The PIC18F2420 has 16 Kbytes of Flash, no EEPROM, and 768 bytes of data RAM. The PIC18F2220 has 4 Kbytes of Flash, 256 bytes of EEPROM, and 512 bytes of data RAM.

Question 5

(a) Problem 2-11

255 or 0FFH

(b) Problem 2-19

(a) 32 bytes
(b) 80 bytes
(c) 4096 bytes

(c) Problem 2-25

Maximum size of the file register / Maximum size of a bank = 4096/256 = 16

(d) Problem 2-26

4096 bytes